PATENT
Docket No. 2207/861502

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS : SHARMA, Vinod Assignee: Intel Corporation

CONTINUATION OF:
SERIAL NO. : 09/540,754

FILED : June 23, 2003

FOR : MULTILEVEL CACHE SYSTEM AND METHOD HAVING A MERGED TAG ARRAY TO STORE TAGS FOR MULTIPLE DATA ARRAYS

GROUP ART UNIT : 2186 (anticipated)

EXAMINER : S.C. Elmore (anticipated)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.98(d)

S I R:

Please consider and make of record pursuant to 37 CFR §1.97-1.98 the information previously cited by or submitted to the Office in the prior application(s) relied on for an earlier filing date under 35 USC §120.

The following listing(s) of such information are attached here (check as appropriate):

[X] a. Forms PTO 892 listing information cited by the Office.
[ ] b. Form PTO 1449 or FB-A820 listing information cited to the Office.

The prior application(s) is(are) identified in the application papers and in the enclosed listing (forms).

Consideration and citation of the references are respectfully solicited.

Respectfully submitted,

KENYON & KENYON

Dated: June 23, 2003 By: _____
Kenneth R. Corsello
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Notice of References Cited	Application/Control No. 09/540,754	Applicant(s)/Patent Under R examination SHARMA, VINOD	
	Examiner Stephen C. Elmore	Art Unit 2186	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,649,139	07-1997	Weinreb et al.	711/202
*	B	US-6,223,260	04-2001	Gujral et al.	711/145
*	C	US-5,813,034	09-1998	Castle et al.	711/146
*	D	US-5,802,578	09-1998	Lovett, Thomas D.	711/147
*	E	US-5,796,980	08-1998	Bowles, James E.	711/144
*	F	US-5,699,551	12-1997	Taylor et al.	711/207
*	G	US-5,623,627	04-1997	Witt, David B.	711/122
*	H	US-4,442,487	04-1984	Fletcher et al.	711/122
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Lee et al., "Shared tag for MMU and cache memory," pp 77-80, CAS '97 Proceedings, Vol. 1, IEEE, October 1997.
	V	Lee et al., "Indirectly-compared cache tag memoryusing a shared tag in a TLB," pp 1764-1766, Electronics Letters, Vol. 3, No. 21, October 1997.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No. 09/540,754	Applicant(s)/Patent Under Reexamination SHARMA, VINOD	
	Examiner Stephen C. Elmore	Art Unit 2186	Page 1 of 1

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	A	US-6,122,709	09-2000	Wicki et al.	711/118
	B	US-5,506,967	04-1996	Barajas et al.	711/113
	C	US-5,553,263	09-1996	Kalish et al.	711/120
	D	US-5,692,152	11-1997	Cohen et al.	711/122
	E	US-			
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	K	US-			
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